MJ3260 (SILICON)

HORIZONTAL DEFLECTION SILICON TRANSISTOR

... designed for use in large screen, 21", 23" and 25" color television receivers, using 90° deflection circuits.

- Collector-Emitter Voltage — V_{CER} = 700 Vdc
- Collector Current — I_C = 6.0 Adc
- Fall Time @ I_C = 5.5 Adc — t_f = 0.4 μs (Typ) = 1.0 μs (Max)
- Circuit Information Included — Complete Technical Dissertation on Requirements for Optimum Circuit Performance

6 AMPERE
POWER TRANSISTOR
NPN SILICON
700 VOLTS
80 WATTS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	250	Vdc
Collector-Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	700	Vdc
Collector-Base Voltage	V_{CB}	700	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	6.0	Adc
Base Current	I_B	2.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.64	Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150	°C

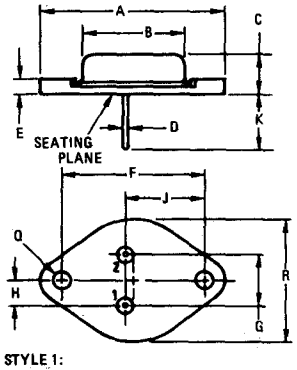
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.56	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	–	–	Vdc
Collector Cutoff Current (V_{CE} = 700 Vdc, V_{BE} = 0)	I_{CES}	–	–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
Collector-Emitter Saturation Voltage (I_C = 5.5 Adc, I_B = 1.25 Adc)	$V_{CE(sat)}$	–	–	6.0	Vdc
Base-Emitter Saturation Voltage (I_C = 5.5 Adc, I_B = 1.25 Adc)	$V_{BE(sat)}$	–	–	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 0.2 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T	–	7.5	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	–	180	pF
SWITCHING CHARACTERISTICS (Figure 1 and text)					
Fall Time (I_C = 5.5 Adc, I_{B1} = 1.25 Adc, L_B = 2.0 μH) R_B = 1.6 Ohms)	t_f	–	0.4	1.0	μs

(1) Pulse Test: Pulse Width 300 μs, Duty Cycle ≈ 2.0%.
(2) $f_T = |h_{fe}| \cdot f_{test}$



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

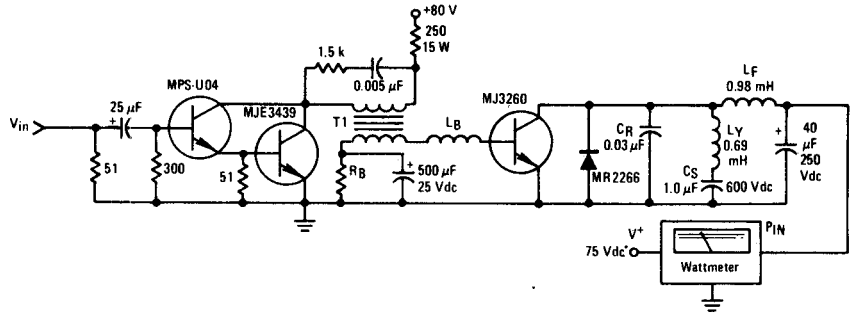
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

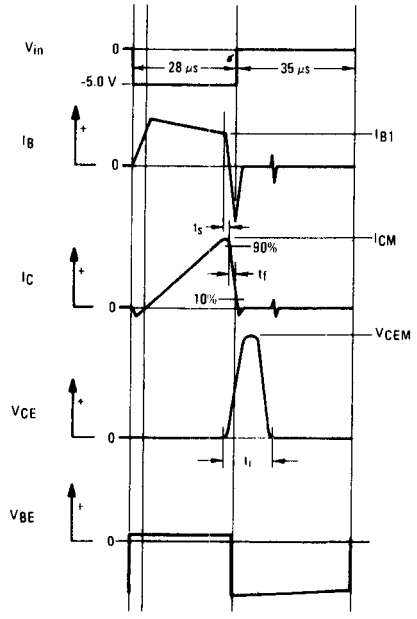
CASE 11

CIRCUIT OPTIMIZATION

Test/application circuit and operating waveforms for MJ3260 are shown in Figure 1. It may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, the circuit was designed with operating efficiency in mind, so that it could be used to evaluate devices by one simple criterion, supply power input. Excessive power input can be caused by a variety of problems, but it is the dissipation itself that is of fundamental importance. Once the transistor operating point has been established, fixed circuit values may be selected for the test fixture. Factory testing may then be made with one meter reading, without adjustment of the test apparatus.

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS





FUNDAMENTAL WAVEFORMS OF A SIMPLIFIED HORIZONTAL DEFLECTION CIRCUIT

DESCRIPTION OF SPECIAL COMPONENTS

DUMMY YOKE INDUCTOR (L_Y)

0.69 mH, 36 turns, #16 AWG enamel wire, 12 turns per layer, 3 layers, 1 mil mylar insulation between layers on 1.3 inch plastic bobbin, enclosed in Ferroxcube cup core No. 4229P3B7, core spacing of 0.006 inch.

DUMMY HIGH VOLTAGE AND HORIZONTAL SCAN TRANSFORMER (L_F)

0.98 mH, 31 turns, #12 AWG enamel wire, 16 turns per layer, 1.9 layers, 1 mil mylar insulation between layers on 2.0 inch plastic bobbin, enclosed in a Ferroxcube cup core K5350-11-3E, core spacing of 0.011 inch.

DRIVER TRANSFORMER (T1)

Motorola part number 25D68782A05-1/4" laminate "E" iron core. Primary Inductance - 39 mH, Secondary Inductance - 0.22 mH, Leakage inductance with primary shorted - 2.0 μH. Primary 260 turns, #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.

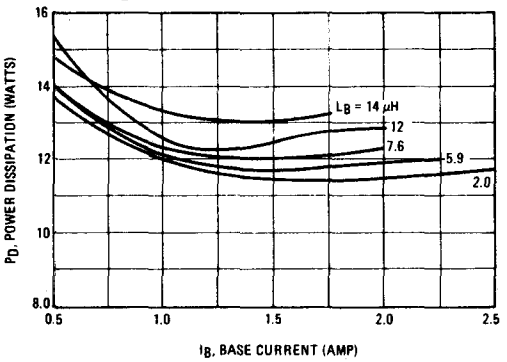
BASIC CONSIDERATIONS

The primary consideration when choosing a deflection transistor for a conventional (parallel connected) circuit, as shown in Figure 1, is one of voltage capability. The flyback voltage to which the device will be subjected is a relatively predictable value with respect to the main power supply voltage. This voltage pulse, (V_{CEM}), shown in Figure 1, will usually be about 8 times the value of V^+, but may be varied somewhat by adjusting retrace time and flyback tuning and can reduce the voltage pulse by 15 to 30% depending on the circuit values chosen.

COLLECTOR CIRCUIT VALUES

The power supply used in the circuit of Figure 1, was chosen to produce a 600 volt collector pulse on the transistor, recommended for regulated applications. The values of yoke (L_Y), flyback primary (L_F), retrace capacitor (C_R), and "S" shaping capacitor (C_S) shown, will result in a peak collector current of about 5.5 A. This is sufficient to deflect (and provide high voltage for) large screen color television receivers using 90° deflection or small and medium-screen color television receivers using 110° deflection. Peak collector currents to 6.0 A may be handled by the MJ3260. Holding the supply constant for most efficient application, adjustment of amount of deflection may be made by raising or lowering L_Y and L_F. Remember that $L_Y I_Y$ is constant for the fixed voltage situation, and actual deflection is proportional to $I_Y \sqrt{L_Y}$. Values of C_S and C_R must be varied inversely with L_Y to maintain retrace and "S" shaping periods.

FIGURE 2 – RELATIONSHIP OF POWER DISSIPATION TO L_B, WITH CHANGING I_{B1}, I_C = 5.5 A PEAK



BASE CIRCUIT VALUES

The driver power supply and driver transistor type can be selected according to convenience. A TO-5 or Uniwatt type will generally be needed. (The Darlington arrangement of the driver transistors used in Figure 1, produces a wide range of I_{B1} current values). Once the driver circuitry is chosen, the turns ratio of the driver transformer can be picked to produce about 4 to 5 volts peak to peak at the base of the output device. Tight coupling between windings is recommended on early designs to allow optimizing leakage inductance by adding inductance externally. Later, the leakage can be "designed in" to the transformer. The R_B and its bypass electrolytic, often called the "speed up" circuit, allows adjustment of I_{B1} (or I_B "end of scan" or I_B end) while still providing a low ac impedance for good turn-off of the output device. In Figure 2, the effects of varying L_B and I_{B1} on the total power input to the deflection circuit are shown. Note that an optimum L_B can be found which will produce low dissipation over a wide range of I_{B1}. This is desirable in order to produce efficient operation over a wide range of circuit component tolerances. Likewise, best L_B also gives the least sensitivity to output transistor h_{FE}.

The best value of L_B found in Figure 2 is 2.0 μH, which is the leakage inductance value of the driver transformer, and no external L is necessary. A lower L_B would have reduced the power dissipation, over a narrow range of I_{B1}. However, a leakage inductance of 2.0 μH is a minimum practical value. The best value of I_{B1} is 2.0 A achieved in the typical device by using R_B = 1.6 Ω, derived experimentally.

These are the choices recommended for the test fixture, when the transistor is used at I_{CM} = 5.5 A. For other values of I_{CM} the drive circuit components must be changed. Figure 3 shows the values of L_B and I_{B1} which should be used. The value of R_B which will be required to produce the corresponding I_{B1} is also given, but of course, it is not an independent variable.

PERFORMANCE

Shown in Figures 4 and 5 are the results which will be typically obtained with the test circuit at various operating conditions.

FIGURE 3 – INTERRELATION OF R_B, L_B, AND I_{B1}

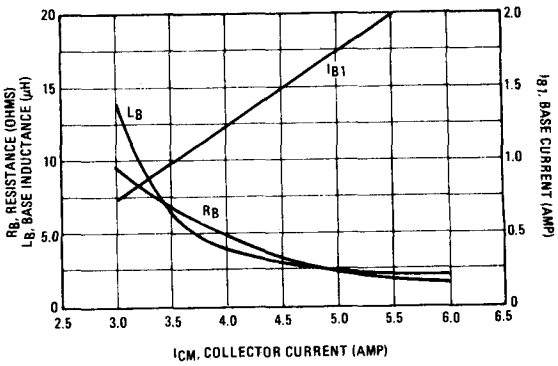


FIGURE 4 – INTERRELATION OF t_f, FALL TIME AND t_s, STORAGE TIME

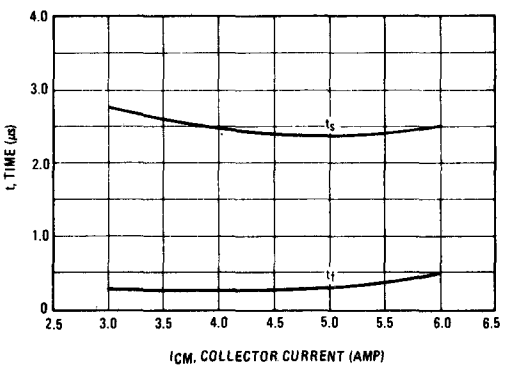
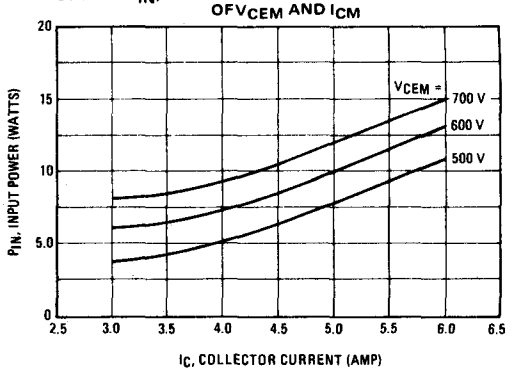


FIGURE 5 – P_{IN}, POWER DISSIPATION WITH DEVIATIONS OF V_{CEM} AND I_{CM}



TYPICAL TRANSISTOR CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

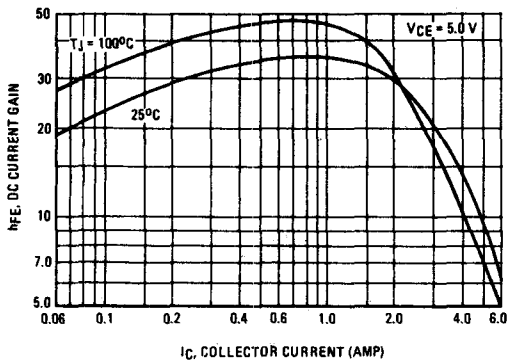


FIGURE 2 – "ON" VOLTAGE

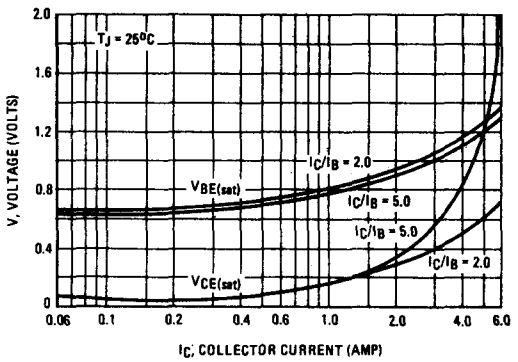
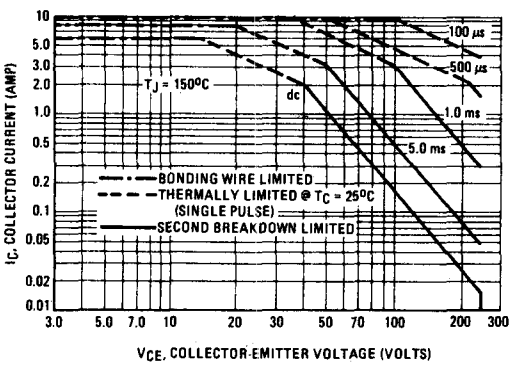


FIGURE 3 – SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415).

FIGURE 4 – TEMPERATURE COEFFICIENTS