

T-33-15

**MOTOROLA**  
**SEMICONDUCTOR**  
TECHNICAL DATA

**Designers Data Sheet**

**SWITCHMODE SERIES**  
**NPN SILICON POWER TRANSISTORS**

The MJ8504 and MJ8505 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

**Fast Turn-Off Times**

- 75 ns Inductive Fall Time -25°C (typ)
- 150 ns Inductive Crossover Time -25°C (typ)
- 1.25 μs Inductive Storage Time -25°C (typ)

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:

- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

**MJ8504**  
**MJ8505**

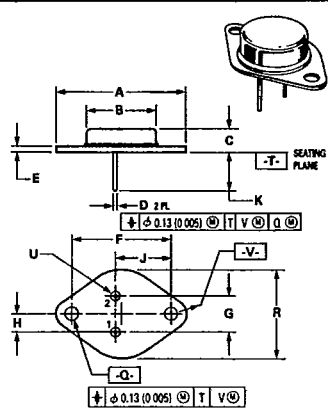
10 AMPERE

**NPN SILICON**  
**POWER TRANSISTORS**

700 and 800 VOLTS  
175 WATTS

**Designer's Data for**  
**"Worst Case" Conditions**

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data - representing device characteristics boundaries - are given to facilitate "worst case" design.



- NOTES:  
1. DIMENSIONS G AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.  
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO 204AA OUTLINE SHALL APPLY.

DIM	MILLIMETERS			INCHES	
	MIN	MAX	MIN	MAX	
A	—	29.27	—	1.550	
B	—	21.08	—	0.830	
C	6.35	8.25	0.250	0.325	
D	0.97	1.09	0.038	0.043	
E	1.40	1.77	0.055	0.070	
F	39.15 BSC		1.187 BSC		
G	10.92 BSC		0.430 BSC		
H	5.46 BSC		0.215 BSC		
J	16.89 BSC		0.665 BSC		
K	11.18	12.19	0.440	0.480	
Q	3.84	4.19	0.151	0.165	
R	—	26.67	—	1.050	
U	4.83	5.33	0.190	0.210	
V	3.84	4.19	0.151	0.165	

STYLE 1:  
PIN 1. BASE  
2. EMITTER  
CASE COLLECTOR

CASE 1-06  
TO-204AA  
(TO-3)

**MAXIMUM RATINGS**

Rating	Symbol	MJ8504	MJ8505	Unit
Collector-Emitter Voltage	V <sub>CEO</sub>	700	800	Vdc
Collector-Emitter Voltage	V <sub>CEV</sub>	1200	1400	Vdc
Emitter Base Voltage	V <sub>EB</sub>	8.0	8.0	Vdc
Collector Current - Continuous	I <sub>C</sub>	10	10	Adc
Peak (1)	I <sub>CM</sub>	15	15	
Base Current - Continuous	I <sub>B</sub>	8	8	Adc
Peak (1)	I <sub>BM</sub>	12	12	
Total Power Dissipation @ T <sub>C</sub> = 25°C	P <sub>D</sub>	175	175	Watts
@ T <sub>C</sub> = 100°C		100	100	
Derate above 25°C		1.0	1.0	W/°C
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-65 to +200		°C

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R <sub>θJC</sub>	1.0	°C/W
Maximum Lead Temperature for Soldering	T <sub>L</sub>	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.

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**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector-Emitter Sustaining Voltage (Table 1) ( $I_C = 100\text{ mA}$ , $I_B = 0$ )	MJ8504 MJ8505 $V_{CE0(sus)}$	700 800	—	—	Vdc
Collector Cutoff Current ( $V_{CEV} = \text{Rated Value}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CEV} = \text{Rated Value}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEV}$	—	—	0.25 5.0	mAdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEV}$ , $R_{BE} = 50\ \Omega$ , $T_C = 100^\circ\text{C}$ )	$I_{CER}$	—	—	5.0	mAdc
Emitter Cutoff Current ( $V_{EB} = 7.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	—	1.0	mAdc

**SECOND BREAKDOWN**

Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			

**ON CHARACTERISTICS (1)**

DC Current Gain ( $I_C = 1.5\text{ Adc}$ , $V_{CE} = 5.0\text{ Vdc}$ )	$h_{FE}$	7.5	—	—	—
Collector-Emitter Saturation Voltage ( $I_C = 5.0\text{ Adc}$ , $I_B = 2.0\text{ Adc}$ ) ( $I_C = 10\text{ Adc}$ , $I_B = 4.0\text{ Adc}$ ) ( $I_C = 5.0\text{ Adc}$ , $I_B = 2.0\text{ Adc}$ , $T_C = 100^\circ\text{C}$ )	$V_{CE(sat)}$	—	—	2.0 5.0 3.0	Vdc
Base-Emitter Saturation Voltage ( $I_C = 5.0\text{ Adc}$ , $I_B = 2.0\text{ Adc}$ ) ( $I_C = 5.0\text{ Adc}$ , $I_B = 2.0\text{ Adc}$ , $T_C = 100^\circ\text{C}$ )	$V_{BE(sat)}$	—	—	1.5 1.5	Vdc

**DYNAMIC CHARACTERISTICS**

Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f_{test} = 1.0\text{ kHz}$ )	$C_{ob}$	90	—	450	pF
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**SWITCHING CHARACTERISTICS**

Resistive Load (Table 1)						
Delay Time	$(V_{CC} = 500\text{ Vdc}$ , $I_C = 5.0\text{ A}$ , $I_{B1} = 2.0\text{ A}$ , $V_{BE(off)} = 5.0\text{ Vdc}$ , $t_p = 50\ \mu\text{s}$ , Duty Cycle $< 2.0\%$ )	$t_d$	—	0.050	0.20	$\mu\text{s}$
Rise Time		$t_r$	—	0.175	2.0	$\mu\text{s}$
Storage Time		$t_s$	—	1.25	4.0	$\mu\text{s}$
Fall Time		$t_f$	—	0.60	2.0	$\mu\text{s}$
Inductive Load, Clamped (Table 1)						
Storage Time	$(I_C = 5.0\text{ A(pk)}$ , $V_{clamp} = 500\text{ Vdc}$ , $I_{B1} = 2.0\text{ A}$ , $V_{BE(off)} = 5\text{ Vdc}$ , $T_C = 100^\circ\text{C}$ )	$t_{sv}$	—	1.75	5.5	$\mu\text{s}$
Crossover Time		$t_c$	—	0.400	2.0	$\mu\text{s}$
Storage Time	$(I_C = 5.0\text{ A(pk)}$ , $V_{clamp} = 500\text{ Vdc}$ , $I_{B1} = 2.0\text{ A}$ , $V_{BE(off)} = 5\text{ Vdc}$ , $T_C = 25^\circ\text{C}$ )	$t_{sv}$	—	1.25	—	$\mu\text{s}$
Crossover Time		$t_c$	—	0.150	—	$\mu\text{s}$
Fall Time		$t_{fi}$	—	0.075	—	$\mu\text{s}$

(1) Pulse Test: PW - 300  $\mu\text{s}$ , Duty Cycle  $< 2\%$ .

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FIGURE 1 - DC CURRENT GAIN

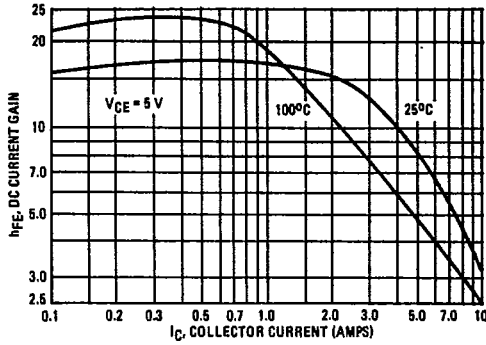


FIGURE 2 - COLLECTOR SATURATION REGION

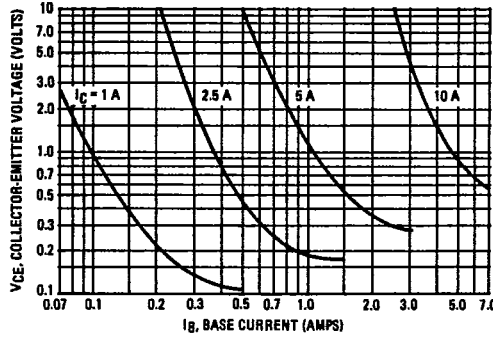


FIGURE 3 - COLLECTOR-EMITTER SATURATION REGION

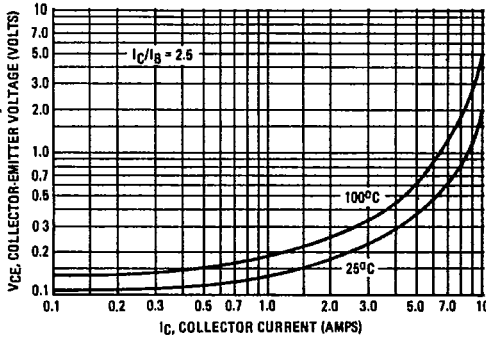


FIGURE 4 - BASE-EMITTER VOLTAGE

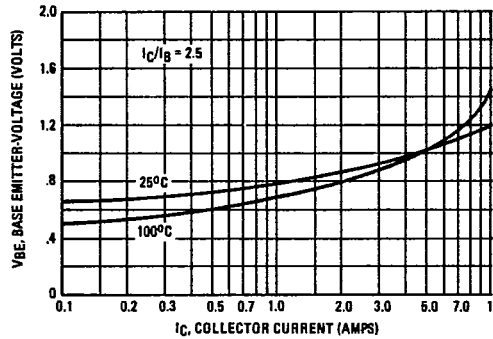


FIGURE 5 - COLLECTOR CUTOFF REGION

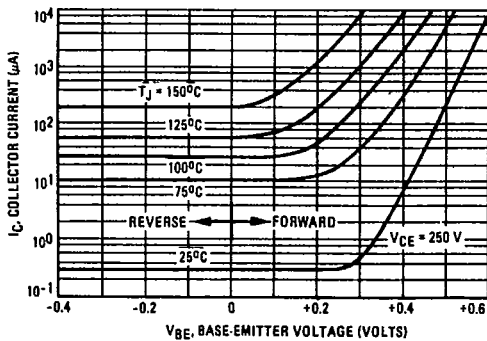
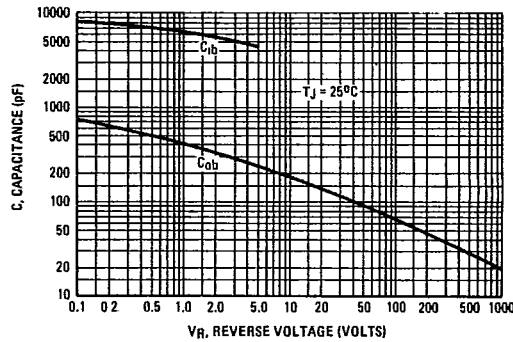


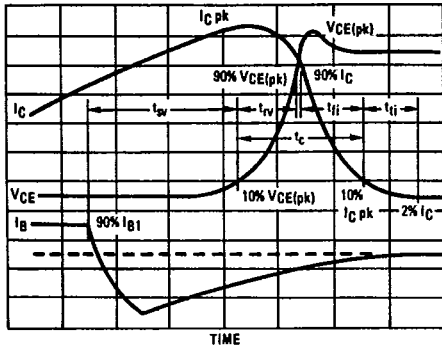
FIGURE 6 - CAPACITANCE



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SWITCHING TIMES NOTE

FIGURE 7 - INDUCTIVE SWITCHING MEASUREMENTS



In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- $t_{sv}$  = Voltage Storage Time, 90%  $I_{B1}$  to 10%  $V_{CE(pk)}$
- $t_{rv}$  = Voltage Rise Time, 10-90%  $V_{CE(pk)}$
- $t_{fj}$  = Current Fall Time, 90-10%  $I_C$
- $t_{ti}$  = Current Tail, 10-2%  $I_C$
- $t_c$  = Crossover Time, 10%  $V_{CE(pk)}$  to 10%  $I_C$

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

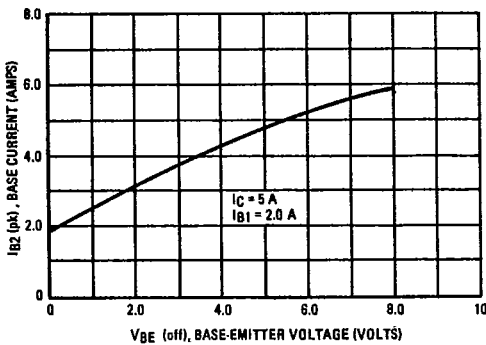
$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general,  $t_{rv} + t_{fj} \approx t_c$ . However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds ( $t_c$  and  $t_{sv}$ ) which are guaranteed at 100°C.

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FIGURE 8 - PEAK REVERSE BASE CURRENT



RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 - TURN-ON SWITCHING TIMES

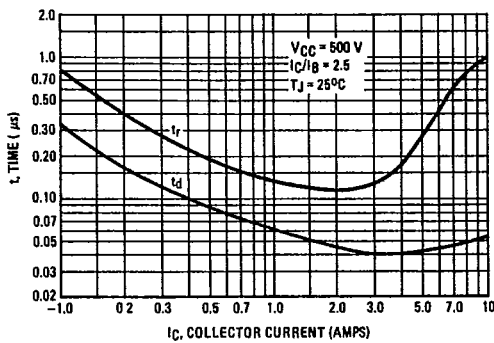


FIGURE 10 - TURN-OFF SWITCHING TIMES

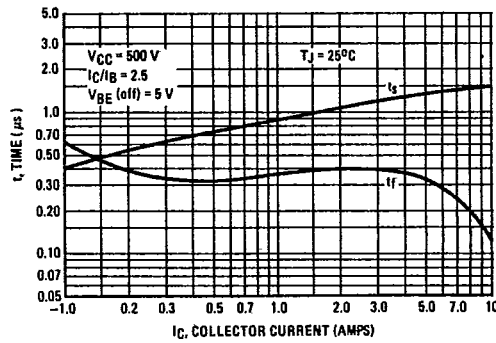


TABLE 1 - TEST CONDITIONS FOR DYNAMIC PERFORMANCE

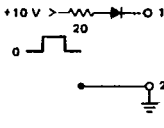
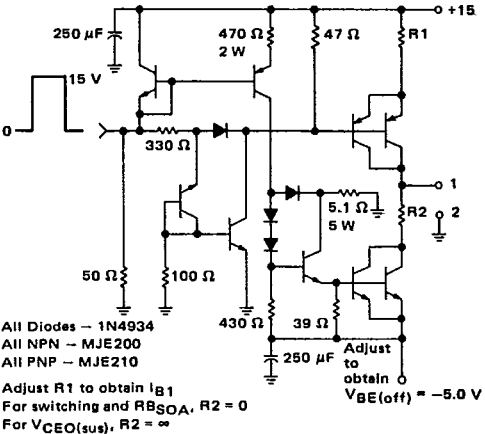
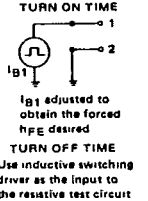
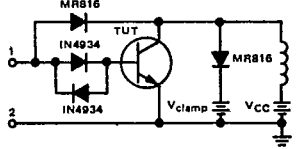
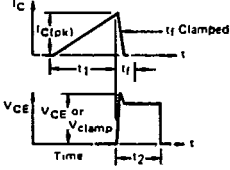
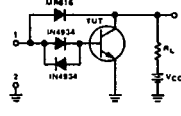
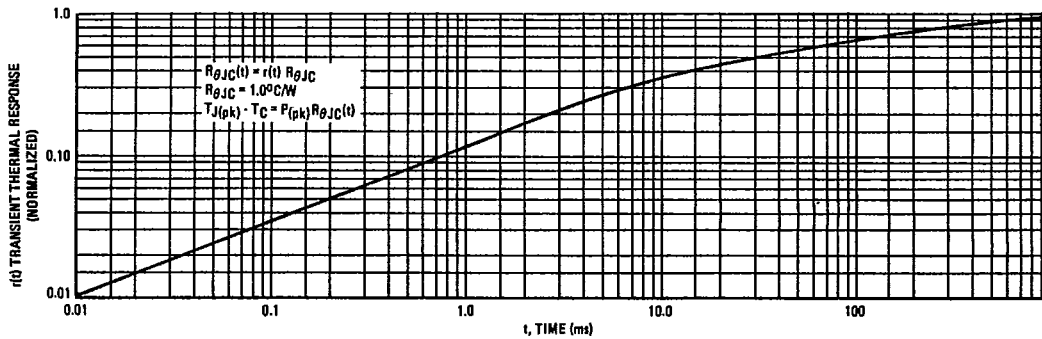
	V <sub>CEO(sus)</sub>	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>+10 V 0 20 PW Varied to Attain I<sub>C</sub> = 100 mA.</p>	 <p>All Diodes - 1N4934 All NPN - MJE200 All PNP - MJE210 Adjust R1 to obtain I<sub>B1</sub> For switching and R<sub>BSOA</sub>, R2 = 0 For V<sub>CEO(sus)</sub>, R2 = ∞</p>	 <p>TURN ON TIME I<sub>B1</sub> I<sub>B1</sub> adjusted to obtain the forced h<sub>FE</sub> desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit</p>
CIRCUIT VALUES	L <sub>coil</sub> = 80 mH V <sub>CC</sub> = 10 V R <sub>coil</sub> = 0.7 Ω	L <sub>coil</sub> = 180 µH R <sub>coil</sub> = 0.05 Ω V <sub>CC</sub> = 20 V V <sub>clamp</sub> = 500 V	V <sub>CC</sub> = 500 V R <sub>L</sub> = 100 Ω Pulse Width = 50 µs
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> 	<p>OUTPUT WAVEFORMS</p>  <p>t<sub>1</sub> Adjusted to Obtain I<sub>C</sub> t<sub>1</sub> = <math>\frac{L_{coil}(I_{Cpk})}{V_{CC}}</math> t<sub>2</sub> = <math>\frac{L_{coil}(I_{Cpk})}{V_{clamp}}</math> Test Equipment Scope - Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 

FIGURE 11 - THERMAL RESPONSE



T-3375  
 T-91-01

SAFE OPERATING AREA INFORMATION

FIGURE 12 - FORWARD BIAS SAFE OPERATING AREA

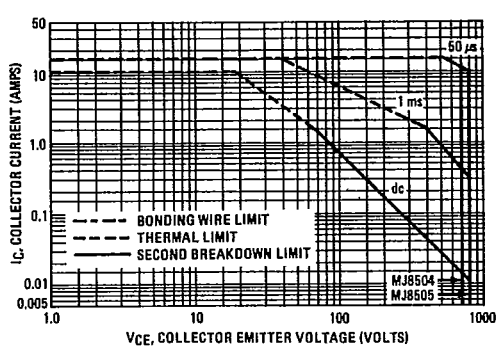


FIGURE 13 - RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA

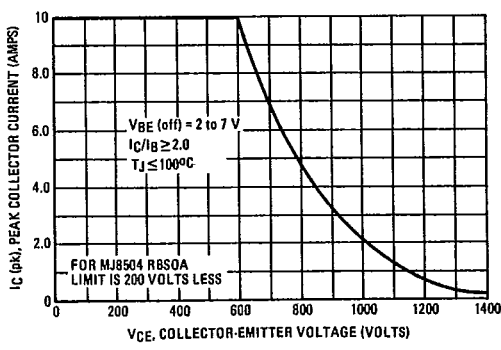
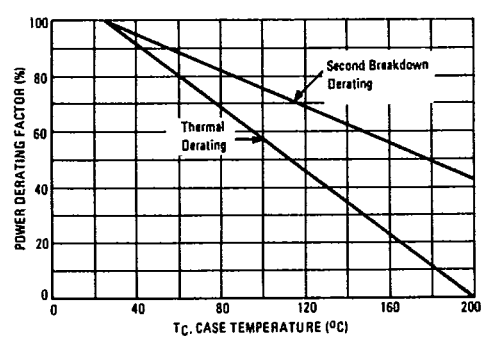


FIGURE 14 - POWER DERATING



FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on  $T_C = 25^\circ\text{C}$ ;  $T_J(\text{pk})$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \geq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(\text{pk})$  may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

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